ABSTRACT OF THE DISCLOSURE

[0034] The invention includes semiconductor processing patterning methods and semiconductor constructions. A semiconductor processing patterning method includes forming a second composition resist layer over a different first composition resist layer. Overlapping portions of the first and second composition resist layers are exposed to actinic energy effective to change solubility of the exposed portions versus the unexposed portions of each of the first and second composition resist layers in a developer solution. The first and second composition resist layers are developed with the developer solution under conditions effective to remove the exposed portions of the first composition resist layer at a faster rate than removing the exposed portions of the second composition resist layer. Additional aspects and implementations are contemplated.